AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1-37. (Canceled)

38. (Currently amended) A semiconductor device comprising:

a substrate having a semiconductor layer and a trench, said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions;

an element isolating insulating film provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a top surface of said semiconductor layer, wherein the element isolation insulating film is an oxide film; and

a MOS type element formed within a corresponding one of the element regions and having a gate insulating film and a gate electrode on the gate insulating film, wherein:

a difference in height from the substrate between a top surface position of said element isolating insulating film and a top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film, the top surface position of said element isolating insulating film is not higher than a top surface position of the gate

electrode, said element isolating insulating film and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer, said element isolating insulating film further having a side surface projecting above the top surface of said semiconductor layer wherein the side surface is substantially perpendicular to the top surface of said semiconductor layer, the gate electrode is formed on the gate insulating film, said gate insulating film being formed on [[a]] the top surface of semiconductor layer in each of said element regions which is not covered with said element isolating insulating film, and said gate electrode is formed on said gate insulating film.

39. (Currently amended) A semiconductor device comprising:

a substrate having a semiconductor layer and a trench, said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions;

an element isolating insulating film provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a top surface of said semiconductor layer, wherein the element isolation insulating film is an oxide film; and

a MOS type element formed within a corresponding one of the element regions and having a gate insulating film, wherein:

a difference in height from the substrate between a top surface position of said element isolating insulating film and a top surface position of said semiconductor layer is at least 10 nm, the top surface position of said element isolating insulating film is not higher than a top surface position o a gate electrode, said element isolating insulating film and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer, said element isolating insulating film further having a side surface projecting above the top surface of said semiconductor layer wherein the side surface is substantially perpendicular to the top surface of said semiconductor layer, the gate electrode is formed on the gate insulating film, said gate insulating film being formed on [[a]] the top surface of semiconductor layer in each of said element regions which is not covered with said element isolating insulating film, and said gate electrode is formed on said gate insulating film.

40. (New) The semiconductor device according to claim 38, wherein the gate electrode contacts the side surface of said element isolating insulating in vertical cross-section perpendicular to a gate length direction of the MOS type element.

41. (New) The semiconductor device according to claim 39, wherein the gate electrode contacts the side surface of said element isolating insulating in vertical cross-section perpendicular to a gate length direction of the MOS type element.